PATENT APPLICATION
Docket No. 5038-340 (P18190)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Pete D. Vogt
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RESPONSE TO NOTICE OF NON-COMPLIANT APPEAL BRIEF

In response to the Notice of Non-Compliant Appeal Brief (37 CFR 41.37) dated October 10, 2007, please amend the Appeal Brief as follows.

Summary of Claimed Subject Matter as required by 37 CFR 41.37(c)(1)(v) begins on page 2.

Remarks begin on page 4.

An **Appendix** listing the claims begins on page 5 of this paper.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 (from which appealed claims 2-5 and 7 depend) is drawn to a memory agent including a receive link interface, a transmit link interface, and a loop back unit coupled to the receive link interface and a transmit link interface. An example embodiment of such a memory agent is described in the substitute specification at page 35, lines 5-13 and illustrated in Fig. 32. The loop back unit may selectively redirect one or more of the receive lanes to one or more of the transmit lanes to retransmit the received training sequences as the return sequences during a lane testing operation (for example, see substitute specification, page 35, lines 10-16).

Claim 2 depends from claim 1 and is drawn to the memory agent of claim 1, further including a second transmit link interface having a plurality of second transmit links and a second receive link interface having a plurality of second receive links. Exemplary embodiments of the recited limitations are disclosed, for example, in the substitute specification at page 23, lines18-30 and illustrated, for example, in Figure 24, where the inner port 136 of the memory agent 134 includes a receive and a transmit link interfaces 140 and 142 respectively, and lanes in the links 54A and 56B implement the recited first receive lanes and first transmit lanes respectively. And the outer port 138 includes second receive and second transmit link interfaces 144 and 146 respectively, and lanes in the links 56A and 56B implement the recited second receive lanes and second transmit lanes respectively.

Claim 3 depends from claim 2 and recites a passthrough mode during a lane testing operation by retransmitting training sequences received on the first receive link interface to the second transmit link interface, and retransmitting return sequences received on the second receive link interface to the first transmit link interface. Such a passthrough mode is disclosed in the substitute specification, for example, at page 36, lines 9-13.

Claim 4 depends from claim 1 and recites that the memory agent may selectively map one of the receive lanes to more than one of the transmit lanes during a lane testing operation. Thus, in an exemplary embodiment such as that described in page 32, lines 2-5 of the substitute specification and illustrated in Figure 32, a training sequence may make a round trip from a memory controller to the memory agent, through a loopback unit in the memory agent (as recited in claim 1), and then back to the memory controller. The loopback unit 196 of Figure 32 may selectively map one of the receive lanes (incoming lanes coupled to the receive link interface 140) to more than one of the transmit lanes (outgoing lanes coupled to the transmit link interface

142) during a lane testing operation. Note that the recited selective mapping occurs inside the memory agent 134 of Figure 32 and is performed by the loopback unit.

Claim 5 depends from claim 1 and recites that the memory agent may selectively map one or more of the first receive lanes to one or more of the second transmit lanes according to a plurality of mappings. Figure 32 (and page 35, lines 5-16 of the substitute specification) discloses an exemplary embodiment of a memory agent with receive lanes mapped to transmit lanes according to a plurality of mapping disclosed, for example, in Figure 33 and page 35, lines 20-27 of the substitute specification.

Claim 7 depends from claim 1 and recites that the memory agent may retransmit the received training sequence with modification as the return sequence. As disclosed in the substitute specification, for example page 36, lines 9-13, the memory agent may retransmit most of the training sequence as the return sequence while modifying only a small group within the sequence to provide identifying or status information to the memory host.

Claim 12 is drawn to a memory agent comprising a first link interface having a plurality of first lanes and a second link interface having a plurality of second lanes. In one embodiment, the memory agent may be a memory controller. The memory agent may transmit training sequences having different mapping indicators to one or more of the plurality of first lanes, as disclosed in the substitute specification, page 35, lines 28-29. The memory agent may receive and analyze the return sequence to identify failed bit lanes, as disclosed in the substitute specification at page 35, lines 15-17.

Claim 17 depends from claim 12 and recites a memory agent transmitting electrical stress patterns in the training sequences. Such electrical stress pattern is disclosed, for example, in the substitute specification at page 30, lines 28-30 and page 31, lines 1-3.

REMARKS

In the Notice of Non-Compliant Appeal Brief (37 CFR 41.37) dated October 10, 2007, the appeal brief filed on May 14, 2007 and the Response to Notice of Non-Compliant Appeal Brief filed July 11, 2007 is objected to for an informality in the concise Summary of the Claimed Subject Matter ("Claim 17 depends from claim 17" should read "Claim 17 depends from claim 12"), and for incorrect designation of the status of claims in the Claims Appendix.

Accordingly, Applicant provides an amended summary of the claimed subject matter, and a replacement Claims Appendix.

CONCLUSION

Applicant requests that the appeal brief submitted earlier be considered and the rejection of claims 2-5, 7, 12 and 17 be reversed.

The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case. Applicant's representative can frequently be reached at (503) 880-3613 outside of normal office hours.

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Respectfully submitted,

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CLAIMS APPENDIX

1. (Previously Presented) A memory agent comprising:

a receive link interface having a plurality of receive lanes to receive training sequences;

a transmit link interface having a plurality of transmit lanes to transmit return sequences; and

a loopback unit coupled to the receive and transmit link interfaces to selectively redirect one or more of the receive lanes to one or more of the transmit lanes to retransmit the received training sequences as the return sequences during a lane testing operation.

2. (Previously Presented) The memory agent according to claim 1 wherein:

the receive link interface is a first receive link interface;

the transmit link interface is a first transmit link interface; and further comprising:

a second transmit link interface having a plurality of second transmit lanes; and

a second receive link interface having a plurality of second receive lanes.

3. (Previously Presented) The memory agent according to claim 2 wherein

the memory agent may operate in a passthrough mode during a lane testing operation by retransmitting training sequences received on the first receive link interface to the second transmit link interface, and retransmitting return sequences received on the second receive link interface to the first transmit link interface.

4. (Previously Presented) The memory agent according to claim 1 wherein the memory agent may selectively map one of the receive lanes to more than one of the transmit lanes during a lane testing operation.

5. (Previously Presented) The memory agent according to claim 1 wherein the memory agent may selectively map one or more of the receive lanes to one or more of the transmit lanes according to a plurality of mappings.

6. (Previously Presented) The memory agent according to claim 5 wherein the memory agent may select one of the mappings responsive to a mapping indicator in a training sequence received on the receive link interface.

7. (Previously Presented) The memory agent according to claim 1 wherein the memory agent may retransmit the received training sequence with modification as the return sequence.

8. (Previously Presented) The memory agent according to claim 1 wherein the memory agent comprises a memory buffer.

9. (Previously Presented) The memory agent according to claim 1 wherein the memory agent comprises a memory module.

10. (Cancelled)

11. (Previously Presented) The memory agent according to claim 1 wherein the loopback unit comprises a multiplexer.

12. (Previously Presented) A memory agent comprising:

a first link interface having a plurality of first lanes; and

a second link interface having a plurality of second lanes;

wherein the memory agent may:

transmit training sequences having different mapping indicators on one or more of the plurality of first lanes;

receive return sequences on one or more of the plurality of second lanes responsive to the training sequences; and

analyze the return sequences to identify failed lanes in the plurality of first lanes and the plurality of second lanes.

13. (Previously Presented) The memory agent according to claim 12 wherein:
the first link interface comprises a receive link interface; and
the second link interface comprises a transmit link interface.

14. (Previously Presented) The memory agent according to claim 12 wherein:
the first lanes comprise receive bit lanes; and
the second lanes comprise transmit bit lanes.

15. (Previously Presented) The memory agent according to claim 12 wherein the memory agent may receive the training sequences as the return sequences.

16. (Previously Presented) The memory agent according to claim 12 wherein the memory agent may transmit test parameters in the training sequences.

17. (Previously Presented) The memory agent according to claim 12 wherein the memory agent may transmit electrical stress patterns in the training sequences.

18. (Previously Presented) The memory agent according to claim 12 wherein the memory agent comprises a memory controller.

19. (Previously Presented) A method comprising:
transmitting a first training sequence to a memory agent on a first plurality of lanes during a testing operation;
transmitting a first return sequence from the memory agent on a second plurality of lanes responsive to the first training sequence according to a first mapping during the testing operation;
transmitting a second training sequence to the memory agent on the first plurality of lanes during the testing operation;
transmitting a second return sequence from the memory agent on the second plurality of lanes responsive to the second training sequence according to a second mapping during the testing operation; and
analyzing the return sequences based on the first and second mappings.

20. (Previously Presented) The method according to claim 19 further comprising:

redirecting the first training sequence to the second plurality of lanes as the first return sequence during the testing operation; and

redirecting the second training sequence to the second plurality of lanes as the second return sequence during the testing operation.

21. (Previously Presented) The method according to claim 20 further comprising:

passing the first training sequence through the memory agent to a third plurality of lanes during the testing operation;

passing the second training sequence through the memory agent to a third plurality of lanes during the testing operation;

passing the first return sequence from a fourth plurality of lanes through the memory agent to the second plurality of lanes during the testing operation; and

passing the second return sequence from the fourth plurality of lanes through the memory agent to the second plurality of lanes during the testing operation.

22. (Previously Presented) The method according to claim 19 wherein the first return sequence comprises one or more groups that are substantially the same as one or more groups in the first training sequence.

23. (Previously Presented) The method according to claim 19 wherein the second return sequence comprises one or more groups that are substantially the same as one or more groups in the second training sequence.

24. (Previously Presented) The method according to claim 19 wherein the first training sequence comprises a mapping indicator.

25. (Previously Presented) The method according to claim 19 wherein the first training sequence comprises an electrical stress pattern.

26. (Previously Presented) The method according to claim 19 wherein the memory agent comprises a memory module.

27. (Previously Presented) The method according to claim 19 wherein the memory agent comprises a memory buffer.

28. (Previously Presented) A memory system comprising:

memory agent comprising:

a receive link interface having a plurality of receive lanes to receive training sequences;

a transmit link interface having a plurality of transmit lanes to transmit return sequences; and

a loopback unit coupled to the receive and transmit link interfaces to selectively redirect one or more of the receive lanes to one or more of the transmit lanes to retransmit the received training sequences as the return sequences during a lane testing operation; and

a memory controller coupled to the memory agent.

29. (Previously Presented) The memory system according to claim 28 wherein:

the first link interface comprises a receive link interface; and

the second link interface comprises a transmit link interface.

30. (Previously Presented) The memory system according to claim 28 wherein:

the first lanes comprise receive bit lanes; and

the second lanes comprise transmit bit lanes.

31. (Previously Presented) The memory system according to claim 28 further comprising a second memory agent coupled to the memory agent.

32. (Previously Presented) The memory agent according to claim 7 wherein the modification includes identifying or status information.

33. (Previously Presented) The memory agent according to claim 1 wherein one of the return sequences comprises one of the received training sequences.

34. (Previously Presented) The memory agent according to claim 1 wherein one of the return sequences consists essentially of one of the received training sequences.